C1 B2

being lost as a result of not being refreshed, said controller operates said DRAM such that a conflicting data access command is satisfied with said memory source other than said memory cells and wherein said memory cells may be refreshed.

C1 B3

47. (Amended) The processor-based system of claim 45, wherein said system for refreshing memory cells further comprises a memory source other than said memory cells such that said controller operates said DRAM such that a conflicting data access command is satisfied with said memory source other than said memory cells and wherein said memory cells may be refreshed.